AM Suppression with Low AM-PM Conversion with the Aid of a Variable-Gain Amplifier

Eric A. M. Klumperink, Carlo T. Klein, Bas Rüggeberg, and Ed J. M. van Tuijl

Abstract—**This paper proposes the use of a variable-gain amplifier instead of a hard limiter for amplitude modulation (AM) suppression with low AM-PM (phase modulation) conversion. A hard limiter shows phase shift variations through input-amplitude dependent changes in output waveform, combined with bandwidth limitations. It is shown that these can be kept small only for limiter bandwidths much larger than the input frequency. A linear amplifier with variable gain used for AM suppression does not suffer from this problem. A CMOS variable-gain amplifier with gain-insensitive phase shift has been designed for this purpose. The benefits and limitations of the technique are explored with reference to an experimental 2.5 μm BICMOS chip for a television IF demodulator. Experimental and simulation results indicate that the AM-PM conversion can be kept below 0.5° at 40 MHz over an input amplitude range of 20 dB, where typical hard limiters show 3–5°. This is achieved with an amplifier bandwidth of 80 MHz, while a hard limiter would need a bandwidth of more than 600 MHz to obtain similar results.**

I. Introduction

LIMITING amplifiers or hard limiters are widely used in broadcasting and communication system receivers. Their basic function is to stabilize the amplitude of a signal, i.e., to suppress amplitude modulation (AM). A limiter should ideally only affect the amplitude of a signal, and be transparent for phase information. In practice, however, limiters exhibit AM-PM conversion (amplitude modulation to phase modulation conversion), which disturbs the phase information. This limits the performance achievable by carrier or clock regeneration circuits and phase demodulators operating under conditions of varying amplitude. In a television IF demodulator as shown in Fig. 1 for instance, the IF signal is demodulated by multiplying it by a constant-amplitude carrier, extracted from the IF input signal by a bandpass filter and a limiter. However, the low-frequency AM behind the bandpass filter disturbs the FM-modulated "intercarrier sound" signal [1] because of the AM-PM conversion of the limiter. Also, in optical communication systems, data-dependent amplitude variations in the clock recovery circuit introduce timing jitter, which increases the bit error rate [2].

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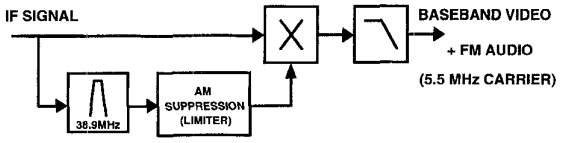

Fig. 1. Block diagram of a TV IF demodulator (PAL, intercarrier sound detection).

Thus, AM suppression circuits with low AM-PM conversion are important for high-performance receivers.

The present paper explores the use of a variable-gain amplifier for AM suppression instead of a hard limiter. It is organized as follows: Section II discusses waveform-dependent phase shifts in hard limiters and the use of a linear amplifier with variable gain to avoid them. In order to acquire a low AM-PM conversion with this approach, an amplifier with a gain-independent phase shift is required. Section III discusses the design of such an amplifier. It is shown that an MOS "Gilbert" multiplier previously described by Geiger *et al.* [3], [4] has the desired phase-shift properties. Section IV identifies several factors that may limit the achievable phase performance of a variable-gain amplifier. First-order design equations are derived to estimate the influence of these factors. Section V deals with the design of an AM suppression circuit for a TV IF demodulator according to the variable-gain concept. Finally, Section VI gives the results of measurements on chips, fabricated in an industrial 2.5 μm BICMOS process, while the overall conclusions drawn from this study are presented in Section VII.

II. Waveform-Dependent Phase Shifts in Hard Limiters and the Use of Variable Gain to Avoid Them

AM is often suppressed using a hard limiter circuit. A practical implementation of such a circuit is a differential pair with a tail current source as shown in Fig. 2(a). The simplified transfer characteristic [Fig. 2(b)] of such a pair can be divided into three parts: a linear region around $V_{in} = 0$, and two saturation or limiting regions for input voltages exceeding the limiting thresholds $\pm V_L$, where I_{out} and thus V_{out} are insensitive to V_{in}, so that the AM information contained in the input signal is suppressed.

Because of the nonlinear nature of the limiter transfer curve, the output waveform differs from that of the input signal. This change of waveform depends on the input

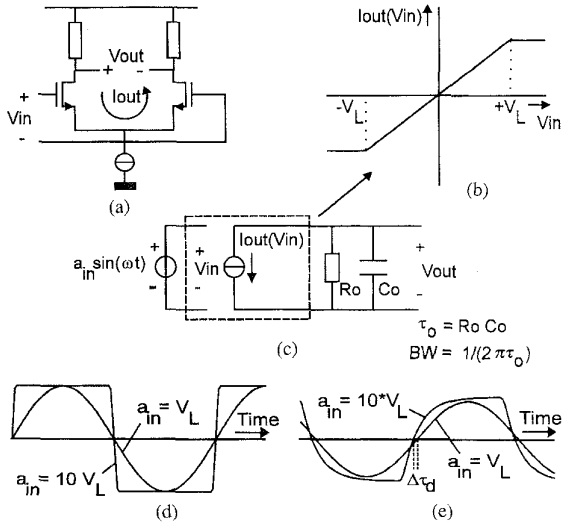

Fig. 2. (a) A practical hard limiter circuit: a differential pair with a tail current source. (b) Simplified transfer characteristic: for input amplitudes $> V_L$ the output amplitude remains constant (AM suppression). (c) Simple model for the transient behavior. (d) Output current I_{out} for $a_{in} = V_L$ and $a_{in} = 10\ V_L$. (e) The resulting output voltage V_{out} for $f_{in}/BW = 0.5$: the difference in delay $\Delta\tau_d$ causes AM-PM conversion.

signal amplitude. In combination with bandwidth limitations, this leads to zero-crossing delay variations, i.e., AM-PM conversion. This can easily be understood with reference to the elementary hard limiter model of Fig. 2(c). If a sinusoidal input signal of amplitude $a_{in} \leq V_L$ is supplied, the limiter has a linear transfer curve and hence a sinusoidal output signal (Fig. 2(d), $a_{in} = V_L$). At larger input amplitudes, the limiter cuts off the peaks of the sine wave, resulting in a trapezoidal and, for very large amplitudes, a square wave-like waveform (Fig. 2(d), $a_{in} = 10\ V_L$). As shown in Fig. 2(e), these waveforms exhibit different zero-crossing delays τ_d when fed through a circuit of finite bandwidth.

For a circuit such as the R-C network of Fig. 2(c) with a single time constant $\tau_o = R_oC_o$, and a bandwidth $BW = 1/(2\pi\tau_o)$, a worst-case estimate of the zero-crossing delay variation $\Delta\tau_d$ can be easily obtained on the assumption that input frequency f_{in} is much smaller than bandwidth BW. Comparing the situations where I_{out} is a sine wave (sinusoidal RC-network response, $\tau_{d,sine} = \tau_o$) and a square wave (exponential RC-network response, $\tau_{d,square} = \tau_o \ln 2$), we find the following expression for the difference in delay

$$\Delta\tau_d = \tau_{d,sine} - \tau_{d,square} = \tau_o - \tau_o \ln 2 \approx 0.3\tau_o \quad (1)$$

where the phase-shift variation is

$$\Delta\varphi = \frac{\Delta\tau_d}{T_{period}} 360^\circ \approx \frac{0.3\tau_o}{1/f_{in}} 360^\circ \approx \frac{f_{in}}{BW} 17.6^\circ. \quad (2)$$

Equation (2) shows that the ratio of bandwidth to input frequency must be high if the phase variation produced by a hard limiter is to be kept low. A more precise analysis of the delay variation $\Delta\tau_d$ assuming a trapezoidal waveform is given in [5]. Fig. 3 shows simulation results ob-

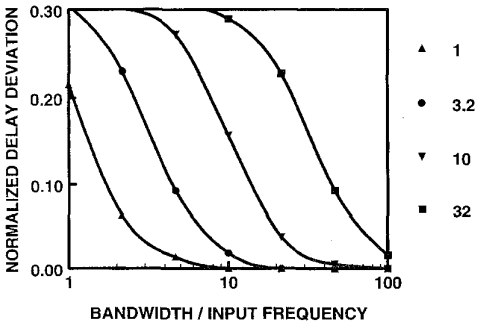

Fig. 3. Normalized delay deviation $(\tau_o - \tau_d)/\tau_o$ of the hard limiter model of Fig. 2(c) as a function of the bandwidth-to-input-frequency ratio for $a_{in}/V_L = 1$, 3.2, 10, and 32.

tained with the model of Fig. 2(c), which are in good agreement with the results of the analysis presented in [5]. The normalized delay deviation $(\tau_o - \tau_d)/\tau_o$ is plotted in this figure as a function of the ratio BW/f_{in} for various values of a_{in}/V_L. We see that as predicted by (1), the delay falls from τ_o for a sine wave ($a_{in}/V_L = 1$, normalized delay deviation = 0) to $0.7\tau_o$ (normalized delay deviation $= 0.3\tau_o$) for large values of a_{in}/V_L (equivalent to a square wave). Fig. 3 also shows how the delay varies between these extreme situations. For instance, for a BW/f_{in} ratio of 10 and a_{in}/V_L varying between 1 and 10, the delay changes by $0.16 \cdot \tau_o$, which results in a phase variation of 0.9° ($0.16 \cdot \tau_o/0.3 \cdot \tau_o$ times the value predicted by (2)).

The analytical expressions derived in [5] can be rewritten and approximated to by the following phase variation expression

$$\Delta\varphi \approx \frac{f_{in}}{BW}\left(e^{-(V_L/a_{in,max})(BW/f_{in})} - 1 - e^{-(V_L/a_{in,max})(BW/f_{in})} - 1\right)57.3^\circ. \quad (3)$$

Fig. 4 shows results calculated with this expression for a_{in}/V_L ranging from 1–10 and 3.2–32, which are in fair agreement with simulation results obtained with the model of Fig. 2(c), also shown in the figure. It can be concluded from Fig. 4 that an increase in input amplitude level has a detrimental effect on the phase variation. Furthermore, in order to keep the phase variation below 0.5° for an amplitude variation of 1 : 10, the ratio BW/f_{in} must be at least 15. If a cascade of low-gain limiters is used, the range of a_{in}/V_L values per stage can be lower, resulting in less phase variation per stage. However, this variation must be multiplied by the number of stages. Furthermore, other sources of phase errors exist in hard limiter circuits. These include slewing limitations, especially in low power/current designs [6], and the bias dependence of the input capacitance of bipolar transistors [2]. Because of the above mentioned problems, it is very hard to achieve a low AM-PM conversion with a hard limiter, and this is only established at high bandwidth-to-input frequency ratios, which come at the expense of considerable power dissipation.

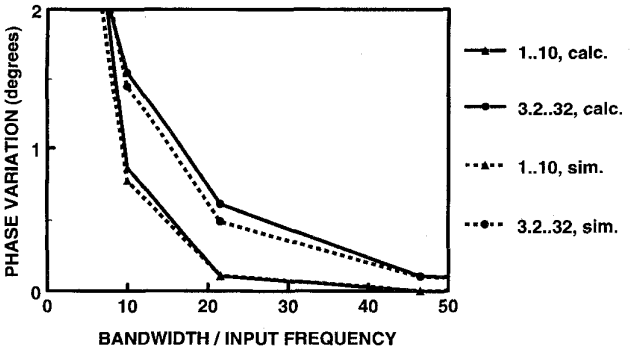

Fig. 4. Calculated (3) and simulated phase variation of the output of the hard limiter of Fig. 2(c) as a function of the bandwidth-to-input-frequency ratio for a_{in}/V_L ranging from 1–10 and from 3.2–32.

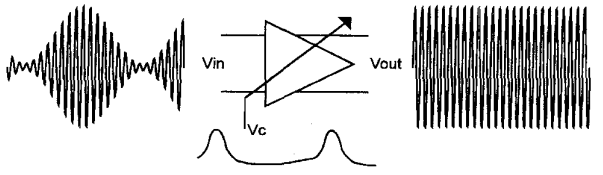

Fig. 5. The principle of AM suppression by means of a variable-gain amplifier.

Bearing in mind that much of the above described AM-PM conversion originates from waveform changes, an obvious solution exists: make sure the waveform does not change. This can be done by using a *linear* variable-gain amplifier instead of the *nonlinear* hard limiter. The basic principle of a variable-gain amplifier used for AM suppression is illustrated in Fig. 5. The AM modulated input signal V_{in} is amplified with a gain that can be controlled by voltage V_c, which is varied in such a way as to ensure that the amplitude of the output signal V_{out} remains constant. If the amplifier has a linear transfer characteristic for a quasi-static control voltage V_c, the output waveform remains a sinusoidal, thus avoiding AM-PM conversion through waveform changes.

An additional advantage of the variable-gain amplifier is that it can handle low-level input signals, unlike the hard limiter where a minimum input amplitude is required to drive the limiter output in saturation. Especially in the case of a full CMOS hard limiter, several hundred millivolts are typically required to saturate the output. This must be multiplied by the ratio of the maximum to minimum amplitude for which the limiter has to be saturated. These fairly large signals must be supplied by a preamplifier circuit to the limiter, which should operate linearly and slew-free to avoid the waveform-dependent delay variations to occur there. It is difficult to satisfy these requirements, especially for low supply voltages.

III. Design of a Variable-Gain Amplifier with Gain-Independent Phase Shift

As discussed in the previous section, use of a variable-gain amplifier can eliminate waveform changes leading to AM-PM conversion. However, in order to be effective,

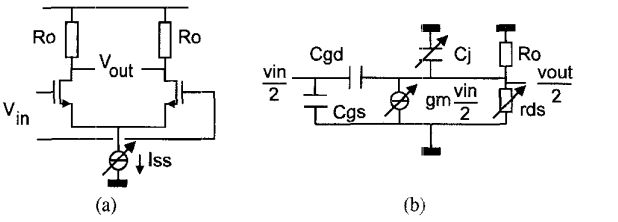

Fig. 6. (a) A differential pair used as a variable-gain amplifier, with I_{ss} as gain controlling parameter and (b) its small-signal equivalent circuit for balanced input signals. (Arrows indicate gain dependencies.)

the amplifier circuit must have a gain-independent phase shift. In general, the gain is varied by changing the bias point of a transistor so that the (trans)conductance that determines the gain changes. Since these conductances also determine the location of the circuit's poles and zeros, this will generally result in a gain-dependent phase shift. However, recent reports of MOS circuits with a gain-insensitive phase shift [7]–[9] suggest that there may be solutions to this problem. These circuits rely on the bias-insensitivity of the gate-source capacitance of a MOST in strong inversion and saturation. Detailed analysis of these circuits shows that gate-drain overlap capacitance currents remain a problem, but can be compensated in cross-coupled topologies. This is best explained starting from the consideration of a simple variable-gain amplifier comprising an MOS differential pair loaded with two resistors as depicted in Fig. 6(a). The gain of this circuit can be varied by means of tail current I_{SS} and is roughly proportional to $\sqrt{I_{ss}}$. If this circuit is driven by small balanced input signals, the common source becomes a virtual ground node. The equivalent circuit of Fig. 6(b) can then be used to represent one half of this circuit, where components whose value varies significantly when I_{SS} is changed are indicated by an arrow. The AC transfer function of this circuit is easily calculated to be

$$\frac{v_{out}}{v_{in}} = -g_m \frac{R_o r_{ds}}{R_o + r_{ds}} \frac{1 - j\omega \dfrac{C_{gd}}{g_m}}{1 + j\omega \dfrac{R_o r_{ds}}{R_o + r_{ds}} (C_{gd} + C_j)}. \quad (4)$$

Equation 4 shows that the low-frequency gain is $g_m R_o$ for $r_{ds} >> R_o$, i.e., the gain varies linearly with g_m. Various effects can be identified introducing gain-dependent (I_{ss} dependent) poles or zeros by inspection of this equation:

1) Transconductance g_m and gate-drain capacitance C_{gd} introduce a zero at g_m/C_{gd} which varies with the gain ($g_m \propto \sqrt{I_{ss}}$).
2) The output resistance r_{ds} of the MOS transistor, which is approximately inversely proportional to I_{SS}, influences the output pole.
3) The value of C_j, which consists largely of the drain-bulk junction capacitances, depends on the output common voltage, which in turn depends on I_{SS}.

Apart from the phase variation problem, a further problem associated with the linear input range of the amplifier

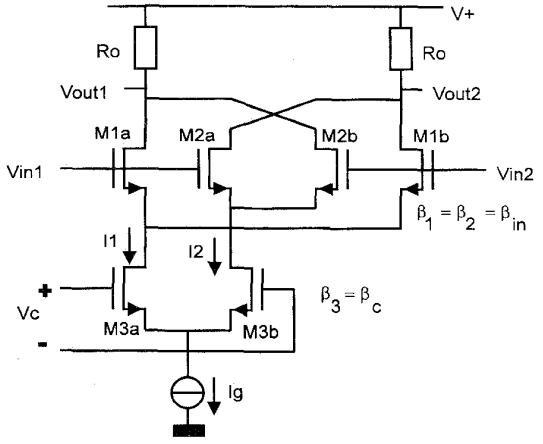

Fig. 7. Variable-gain amplifier with very low phase shift variation.

may arise. The circuit of Fig. 6 has a wide input range for a high gain (large I_{SS}) and a narrow input range for a low gain. This is exactly the opposite of what is required from the variable-gain amplifier: we need a wide input range at low gain, if the input amplitude is large.

Most of the above-mentioned problems are solved when the cross-coupled circuit topology shown in Fig. 7 is used. This circuit was previously described by Geiger *et al.* as a multiplier [3] and is well known in a bipolar transistor version as the Gilbert multiplier [4]. Assuming a square-law MOST characteristic, we find the following relation for the voltage gain A_u [3]

$$A_u = \frac{V_{\text{out}1} - V_{\text{out}2}}{V_{\text{in}1} - V_{\text{in}2}} = -(g_{m1} - g_{m2})R_o$$

$$= -\sqrt{\frac{\beta_{\text{in}}\beta_c}{2}}\, R_o V_c = \alpha_m V_c \qquad (5)$$

where g_{m1} and g_{m2} are the transconductances of the upper differential pairs and β_{in} and β_c are the conversion factors $\mu C_{\text{ox}} W/L$ of the upper and lower MOS transistors respectively. Note that A_u does not depend on I_g: the multiplier output voltage can only be increased by increasing transistor aspect ratios or R_o.

A detailed analysis of the circuit reveals that the previously mentioned effects leading to gain-dependent phase shift no longer apply:

1) The zero due to C_{gd} is compensated in the cross-coupled topology of the upper differential pairs. With balanced input signals, the capacitive current in C_{gd1a} and C_{gs2a} due to $+v_{\text{in}}/2$ is equal to that in C_{gd1b} and C_{gd2b} due to $-v_{\text{in}}/2$, so that $V_{\text{out}1}$ and $V_{\text{out}2}$ remain unchanged.
2) The sum of the currents I_1 and I_2 is constant (equal to I_g), resulting in a constant common-mode output voltage and hence a constant junction capacitance C_j.
3) The two outputs are connected to two drain-source conductances, one from the outer and one from the inner differential pair. Since these conductances are roughly proportional to the bias current, the total output conductance seen at one output node is proportional to the sum of I_1 and I_2, which is constant (equal to I_g).

Apart from these attractive phase properties, the multiplier also has favorable input range properties: at low gain, the upper differential pairs operate at roughly half the value of I_{SS} and thus have a wide input range as desired.

Fig. 8 shows the improvement in phase-shift variation brought about by the topology change, as simulated with the component values of Table I and an input voltage source resistance of 1 K ohm. The phase-shift variation for the cross-coupled topology is less than 0.1° at 40 MHz for a gain range of −15 to +5 dB, while a differential pair with the same components exhibits 25° of phase-shift variation. Even when manufacturing tolerances and mismatch are taken into account, the phase-shift variation remains less than 0.3°.

Although an MOS multiplier is discussed here, a BJT implementation would also be possible. However, bias-dependent C_{be} variations make it more difficult to obtain a very low phase shift here, since they introduce a gain-dependent pole in combination with a source resistance. This effect is negligible for a MOST implementation, since C_{gs} is fairly bias-insensitive here.

IV. Causes of Phase Variations Using Variable Gain

During the evaluation of the variable-gain amplifier, it became clear that several effects can detrimentally affect the desired constancy of the phase shift. The following phenomena appear to be relevant: gate-drain capacitance inequality, distortion, and ripple on the gain-control voltage V_c. First-order models estimating the influence of these effects will now be derived.

A. Gate-Drain Capacitance Inequality

As discussed in Section III, gate-drain capacitances introduce a right-hand half-plane zero, which cancels out in the cross-coupled topology of Fig. 7, as long as the gate-drain capacitances of the MOS transistors in the upper differential pairs are equal. In practice, however, inequalities ΔC_{gd} occur because of transistor mismatches and the bias dependence of C_{gd}.[1] As a result, the zeros do not cancel out completely, and an effective zero is found at

$$f_{\text{zero}} = \frac{g_{m1} - g_{m2}}{2\pi \Delta C_{gd}}. \qquad (6)$$

If the gate-drain capacitances are equal, this zero is located at infinity. If a C_{gd} inequality exists, f_{zero} changes in

[1]In fact, advanced MOST models often include nonreciprocal transcapacitances, which are bias dependent [10]. In that case, the transcapacitance from gate to drain occurs in the expression of f_{zero} instead of C_{gd}.

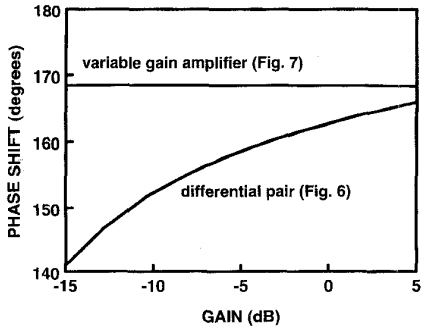

Fig. 8. Simulated phase shift of the variable-gain amplifiers of Figs. 6 and 7 as a function of the gain.

TABLE I
VALUES OF THE MAIN COMPONENT PARAMETERS AND BIASING VARIABLES USED IN SIMULATIONS AND MEASUREMENTS

Component Property	Value
β_{in} (150/5 NMOST)	1.2 mA/V^2
β_c (360/3 NMOST)	4.8 mA/V^2
β_{sq} (200/5 PMOST)	0.4 mA/V^2
$f_{T,max}$ of NPN	5 GHz
f_{Tmax} of (lateral) PNP	10 MHz
R_{sq}	10 Kohm
R_l	2.5 Kohm
R_c	20 Kohm
R_o	3 Kohm
C_l	2 pF

Biasing variable	Value
I_g	500 μA
I_{sq}	250 μA
I_r	2 μA
V_+	8 V
V_{b1}	1.8 V
V_{b2}	3 V

the same ratio as the gain, since the latter is proportional to $g_{m1} - g_{m2}$. For signal frequencies well below f_{zero}, the resulting phase shift variation can be estimated by

$$\Delta\varphi = \Delta \arctan \frac{f_{in}}{f_{zero}} \approx \frac{f_{in}}{\Delta f_{zero}} \frac{360^\circ}{2\pi}$$

$$= f_{in} R_o \Delta C_{gd} \left(\frac{1}{A_{u,\min}} - \frac{1}{A_{u,\max}} \right) 360^\circ \qquad (7)$$

where $A_{u,\min}$ and $A_{u,\max}$ are the minimum and maximum values of the gain given by (5). For a typical C_{gd} mismatch of 3%, (7) predicts a phase shift of 0.3° for the circuit of Fig. 7 with the component values of Table I, which agrees well with simulation results.

B. Distortion

In the above discussion, it was assumed that the variable-gain amplifier has a linear transfer characteristic, so that the output and input signal waveforms are the same. However, a practical variable-gain amplifier will have a finite linearity. In an weakly nonlinear circuit, the second-order and third-order components of this distortion are usually the most important. These components have an effect on the zero-crossing delay of the amplifier and will be analyzed separately. The model used for this purpose is identical with that of Fig. 2(c), except that I_{out} is now given by

$$I_{out} = g_m V_{in} + g_2 V_{in}^2 + g_3 V_{in}^3 \qquad (8)$$

where the second and third terms model the second- and third-order distortion, respectively.

Second-Order Distortion: If a sinusoidal signal $a_{in} \sin(\omega_{in} t)$ is applied to the input and only the second-order term is taken into account ($g_2 \neq 0$, $g_3 = 0$), the output voltage has the form

$$V_{out} = R_0 \left(\frac{1}{2} g_2 a_{in}^2 + g_m a_{in} \frac{\sin(\omega_{in} t - \arctan(\omega_{in}\tau_o))}{\sqrt{1 + \omega_{in}^2 \tau_o^2}} - \frac{1}{2} g_2 a_{in}^2 \frac{\cos(2\omega_{in} t - \arctan(2\omega_{in}\tau_o))}{\sqrt{1 + 4\omega_{in}^2 \tau_o^2}} \right). \qquad (9)$$

Equation (9) indicates that a dc term and second harmonic occur in addition to the fundamental. If ac coupling is assumed, the dc term has no influence. The second harmonic, however, is a cosine function which has its maximum close to the zero crossing of the fundamental. This results in a shift of the zero crossing of V_{out} with respect to the situation without second harmonic. Comparison of these two situations allows the phase difference to be calculated. Assuming small values of the second harmonic distortion HD2 and $\omega_{in} \cdot \tau_o \ll 1$, we find the following simple expression for the phase variation

$$\Delta\varphi_{HD2} \approx \text{HD2} \frac{360^\circ}{2\pi}. \qquad (10)$$

Simulation showed that the above approximations yield less than 20% error for HD2 ≤ 10% and $\omega_{in}\tau_o \leq 0.5$. It follows from (10) that HD2 should be less than 0.9% for a phase-shift variation of less than 0.5°.

Third-Order Distortion: If a sinusoidal signal $a_{in} \sin(\omega_{in} t)$ is applied to the input, and only the third-order term is taken into account ($g_2 = 0$, $g_3 \neq 0$), the output voltage has the form

$$V_{out} = R_0 \left(\left(g_m a_{in} + \frac{3}{4} g_3 a_{in}^3 \right) \cdot \frac{\sin(\omega_{in} t - \arctan(\omega_{in}\tau_o))}{\sqrt{1 + \omega_{in}^2 \tau_o^2}} + \frac{1}{4} g_3 a_{in}^3 \frac{\cos(3\omega_{in} t - \arctan(3\omega_{in}\tau_o))}{\sqrt{1 + 9\omega_{in}^2 \tau_o^2}} \right). \qquad (11)$$

Equation (11) indicates that in addition to the fundamental a third harmonic occurs at the output, with a zero crossing at the same location as that of the fundamental if $3\omega_{in}\tau_o \ll 1$ ($\arctan(3\omega_{in}\tau_o) \approx 3\omega_{in}\tau_o$, linear phase and constant group delay). However, because of the nonlinear phase characteristic, the third harmonic is subject to a different delay than the fundamental, which results again in an HD3-dependent and hence input-amplitude dependent phase variation. If a first-order low-pass filter is assumed the resulting phase variation can be approximated to by the following expression for low values of HD3

$$\Delta\varphi_{HD3} \approx \text{HD3} \arctan \left(3 \frac{f_{in}}{f_{RC}} \right). \qquad (12)$$

In contrast to the second-order distortion case, the phase variation now depends on the ratio of the frequency of the input signal f_{in} to the bandwidth of the RC-network f_{RC}. Simulations showed that the above approximations yield less than 10% error for HD3 $\leq$ 10% and $\omega_{in}\tau_o \leq 0.5$. It follows from (12) that HD3 should be less than 0.9% for $f_{in}/f_{RC} = 0.5$ if a phase shift of less than 0.5° is desired.

C. Ripple on Control Voltage V_c

In order to suppress the AM information of the input signal, the control voltage V_c should vary in step with the envelope of V_{in}. This AM information typically comprises much lower frequencies than those of the input signal. Thus, V_c should only contain these lower-frequency components and none at the carrier or clock frequency to be regenerated. However, since V_c is derived in some way from the input signal, it usually contains some residual at the clock/carrier frequency. Furthermore, if a squaring circuit is used to detect the AM information (see Section V), a second harmonic is also introduced. Since the variable-gain amplifier is essentially a multiplier or mixer, this results in extra coherent signal components and extra distortion at the output.

A coherent output signal is introduced if the signal input of the multiplier exhibits an offset voltage due, e.g., to transistor mismatch. However, simulation shows that this is mainly a common component for V_{out1} and V_{out2} and largely cancels out if the differential output signal is used.

The multiplication of an input signal at frequency ω_{in} with components in V_c at ω_{in} and $2\omega_{in}$ introduces extra second- and third-order distortion products, respectively. The effect of these distortion products on the phase performance was discussed in Section III. On the basis of the above discussion and the calculations in the Section IV-B above, it may be concluded that the ripple on V_c should not introduce a distortion greater than 0.9% if the phase shift is to be kept below 0.5°. It follows that the ripple should typically be less than 1% of V_{C0}, the nominal control voltage.

V. Design of an AM Suppression Circuit for a Television IF Demodulator

In order to evaluate the variable-gain concept an experimental chip was designed in an industrial 2.5 μm BICMOS process. The circuit was designed to fit in an existing television IF demodulator (see Fig. 1). An input amplitude range of 25 mV to 250 mV and a nominal output amplitude of 50 mV were aimed at. The IF frequency is 38.9 MHz and the bandwidth of the AM information is roughly 2 MHz, determined by the bandpass filter preceding the AM suppression circuit (see Fig. 1). A phase error $<0.5°$ is aimed at in order to obtain an acceptable signal-to-buzz ratio with intercarrier sound detection [1]. Simulations on practical bipolar hard-limiter circuits designed in the same BICMOS process and biased at about 1 mA showed a phase shift of 3–5° at the IF frequency of 38.9 MHz over an input amplitude range of 20 dB. MOS hard limiters showed even larger phase shifts. Nevertheless, the simulation results of Fig. 8 indicate that the variable-gain concept can yield phase-shift variations of less than 0.5°.

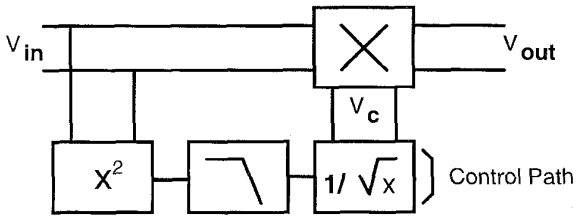

Fig. 9. Block diagram of the variable-gain AM suppression circuit realized on chip.

A block schematic of the AM suppression circuit implemented on chip is given in Fig. 9. For a constant output amplitude, control voltage V_c must be inversely proportional to the amplitude of the input signal. This is accomplished by a gain control path, which basically determines the RMS value of the input signal and adjusts the gain inversely proportional to it. This is implemented by means of a squaring circuit, a low-pass filter, and a circuit supplying the inverse of the square root of its input signal. The squaring circuit produces an output which contains the square of the input amplitude

$$(a_{in}\sin(2\pi f_{in}t))^2 = \tfrac{1}{2}(a_{in}^2 - a_{in}^2\cos(4\pi f_{in}t)). \quad (13)$$

A low-pass filter suppresses the second harmonic in (13), so that the square of the input amplitude is detected. Calculation of the inverse of the square root of this signal gives a control voltage inversely proportional to the input amplitude. With a sinusoidal input voltage $V_{in} = a_{in}\sin(2\pi f_{in}t)$, V_c will be equal to

$$V_c = \frac{\alpha_c}{\sqrt{V_{in}^2}} = \sqrt{2}\,\frac{\alpha_c}{a_{in}} \quad (14)$$

where α_c is a design parameter discussed below, of dimension volt^2. The output voltage of the AM suppression circuit is then given by

$$V_{out} = \alpha_m V_c V_{in} = \alpha_m\alpha_c\sqrt{2}\sin(2\pi f_{in}t) \quad (15)$$

where α_m is given in (5). If both α_m and α_c are constant, the output amplitude is stabilized.

Especially because of the low-pass filter in the gain control path, voltage V_c has a delay with respect to the multiplier input signal. This delay does not affect the AM-PM conversion of the circuit, but does reduce the AM suppression for high frequency AM components [11]. However, by including a suitable delay in the signal path, this problem can be solved, if necessary. For the TV IF demodulator this was not done, since only audio frequency AM components are of concern for hi-fi sound quality.

Fig. 10 shows a more detailed schematic of the circuit implemented on chip. The variable-gain amplifier of Fig.

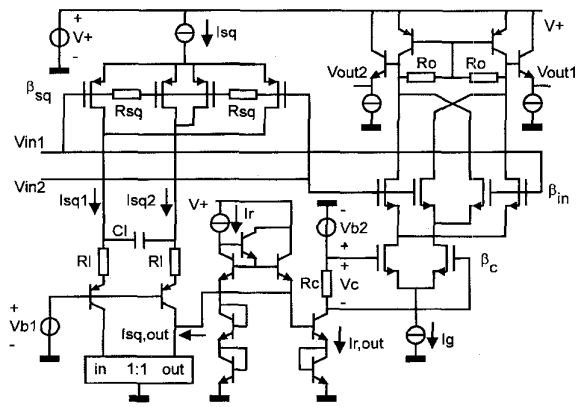

Fig. 10. Detailed schematic of the circuit realized on chip.

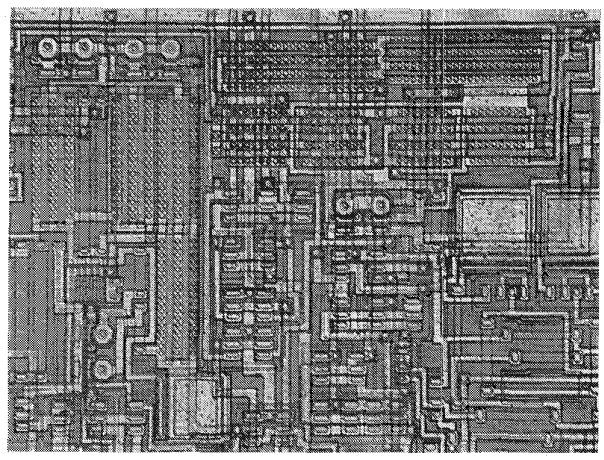

Fig. 11. Chip photograph of the variable-gain AM suppression circuit (450 × 330 μm^2).

7 is biased by current source I_g. PNP transistors above the amplifier absorb the common part of the output currents, while resistors R_o convert the differential part to a differential output voltage. The output voltages V_{out1} and V_{out2} are buffered with NPN emitter followers to bondpads for measurement purposes. The squaring circuit of the control path is implemented by the common source PMOS transistors, bias current source I_{sq}, and resistors R_{sq}. Assuming a square-law $I_d(V_{gs})$ relation, we can easily show that

$$I_{sq,out} = I_{sq1} - I_{sq2} = \tfrac{1}{4}\beta_{sq}(V_{in1} - V_{in2})^2. \quad (16)$$

This result is independent of the source voltage of the MOST's, and thus of the impedance connected to the source, so that a current source can be used to provide the squaring circuit with a floating input. The currents I_{sq1} and I_{sq2} are passed through a current-mode low-pass filter consisting of resistors R_l, capacitance C_l and two PNP transistors and are subtracted in a current mirror. Six NPN transistors connected in a translinear loop, biased by I_r and an NPN transistor operate on the filtered squarer current. This translinear loop, in which the current product of the clockwise and counterclockwise oriented transistors are equal, delivers an output current

$$I_{r,out} = \frac{\sqrt{I_r^3}}{\sqrt{I_{sq,out}}}. \quad (17)$$

Finally, the output current $I_{r,out}$ is converted to the gain-control voltage V_c by R_c. Using (14)–(17), we find design parameter α_c to be given by the expression

$$\alpha_c = 2\sqrt{\frac{I_r^3}{\beta_{sq}}}R_c. \quad (18)$$

Using (5), (14), and (18), we can calculate the amplitude at the output of the AM suppression circuit to be

$$a_{out} = \alpha_c\alpha_m\sqrt{2} = 2\sqrt{\frac{\beta_{in}\beta_c I_r}{\beta_{sq}}}I_r R_c R_o. \quad (19)$$

Equation (19) shows that the output amplitude depends on some design parameters, but also on the current I_r, thus permitting electronic control or correction of the output level.

VI. Measurement Results

The AM suppression circuit for a TV IF demodulator was fabricated in an industrial 2.5 μm BICMOS process (see Fig. 11). A dc test was performed to verify the functional operation of this circuit and to evaluate its AM suppression properties. Fig. 12 shows the results. The output voltage varies from 37 to 40 mV over an input voltage variation of 25–250 mV, which means that the modulation index is reduced by more than a factor of 10. This result agrees fairly well with the simulation results. The remaining variation in V_{out} is mainly due to deviations from square-law behavior of the MOS transistors. The measured distortion of the multiplier was below 1% over the whole input voltage and gain range.

In order to evaluate the phase-shift properties, the ac transfer function of the AM-suppression circuit was measured. RF transformers were used to obtain a balanced input voltage and to measure the differential output voltage. The −3 dB bandwidth of the circuit was 80 MHz, independent of the gain. A plot of the measured and simulated phase (including measurement setup delays) as a function of the gain is shown in Fig. 13 for four chips. This figure shows that the measured phase is not as constant as desired, or as simulated—a phase variation of 5° is found instead of 0.5° over a gain range of 20 dB. However, a closer look at the results shows how this can be explained. Comparison of the results for different chips reveals a strong common systematic effect—the phase shift falls off quite sharply as the gain is decreased. This effect is reproduced in simulations by introducing a ΔC_{gd} in the order of 10 fF (30% of C_{gd}) in the variable-gain amplifier. Detailed inspection of the layout of the chip showed that a large asymmetry in capacitive coupling indeed exists. Furthermore, (7) fits the observed phase variation quite good. By attributing all the phase shift at low gains to C_{gd}

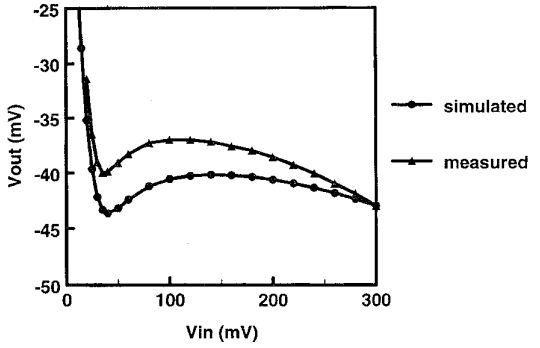

Fig. 12. Measured and simulated dc transfer curves of the AM suppression circuit.

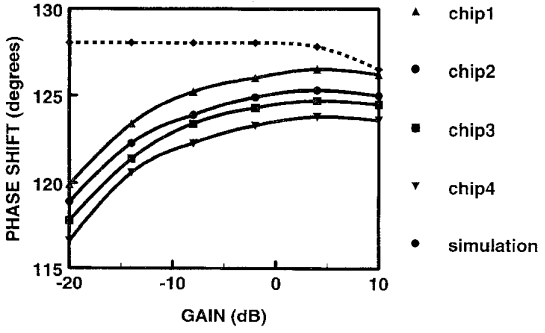

Fig. 13. Measured and simulated phase shift at 40 MHz as a function of the gain for four chips.

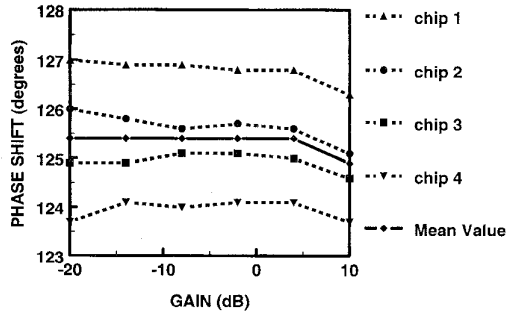

Fig. 14. Compensated results of the phase shift measurements at 40 MHz as a function of the gain for four chips (see text).

differences, a compensated phase curve for every chip was calculated using (7). By first averaging the phase measurement results, a fair estimate for ΔC_{gd} was obtained. The compensated results for the individual chips are shown in Fig. 14, together with their mean value. The phase variation for all chips is now less than 0.4° over a gain range from −15 to +5 dB. The systematic effect that remains can be explained by the bias dependence of C_{gd} as discussed in Section IV-A. If the gain is not increased above +4 dB, the phase variation introduced by this effect remains <0.3° (mean curve). The phase curves of the individual chips show diverse phase variations <0.3° over a gain range of −20 to 0 dB. This can be explained as due to a random C_{gd} mismatch of the order of 3% of C_{gd}. Thus overall a phase variation of less than 0.5° seems feasible at 40 MHz over 20 dB gain variation in a 2.5 μm CMOS process.

VIII. Conclusions

Research has been carried out to explore the possibilities of implementing an AM suppression function with low AM-PM conversion by using a variable-amplifier instead of a hard limiter. In this way, phase variations due to waveform changes in combination with bandwidth limitations are largely eliminated. In order to ensure a low AM-PM conversion, a variable-gain amplifier with a gain-independent phase shift is needed. It is shown that a previously published MOS multiplier [3] is very suitable for this purpose. Effects that may introduce phase errors were identified and quantified in design equations. Gate-drain capacitance inequalities in the MOST multiplier appear to be the main source of phase variations, provided the distortion of the amplifier is low enough. An experimental AM suppression circuit for a TV IF demodulator was designed and fabricated in a 2.5 μm BICMOS process. Simulation and measurement results indicate that an AM modulation index reduction by a factor of 10 and a phase variation of less than 0.5° can be achieved at 40 MHz over a gain range of 20 dB with an amplifier bandwidth of 80 MHz. Hard limiters designed in the same process typically exhibit 3–5° phase shift under these conditions, and would need a bandwidth of more than 600 MHz to achieve similar results.

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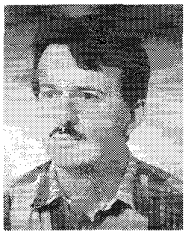

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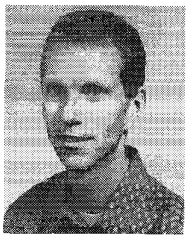

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